DATASHEET

2/17/2023

Fema Part Number

AM450600-24	
Description	2.4” Active Matrix Full Color OLED
	450X600 Resolution
	High Brightness 800 nits (typical)
	Optional Touchpanel Available

Fema Electronics Corporation:

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Please visit our website www.femaelectronics.com or email us at tft@femacorp.com

1. GENERAL INFORMATION

No.	Item	Contents	Unit
1	LCD size	2.4 inch (Diagonal)	/
2	Display mode	Rigid AMOLED	/
3	Viewing direction(eye)	FREE	/
4	Gray scale inversion direction	-	/
5	Resolution(H*V)	450*600 Pixels	/
6	Module size (L*W*H)	38.72*51.56*0.78	mm
7	Active area (L*W)	36.72*48.96	mm
8	Pixel pitch (L*W)	0.0816*0.0816	mm
9	Interface type	MIPI/MCU/SPI interface	/
10	Color Depth	16.7M	/
11	Module power consumption	0.01(Min.),0.45(Max)(Appr)	W
12	Back light type	EDGE&WHITE LED	/
13	Driver IC	RM690B0	/
14	Weight	4(Appr)	G

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT	VDD	-0.3	3.6	V	
Operation temperature	Top	-20	+80	℃	
Storage temperature	Tst	-40	+80	℃	
Humidity	RH	-	90%	RH	Note1

Note1 :

1).The maximum wet bulb temperature ≤40℃ and without dewing.

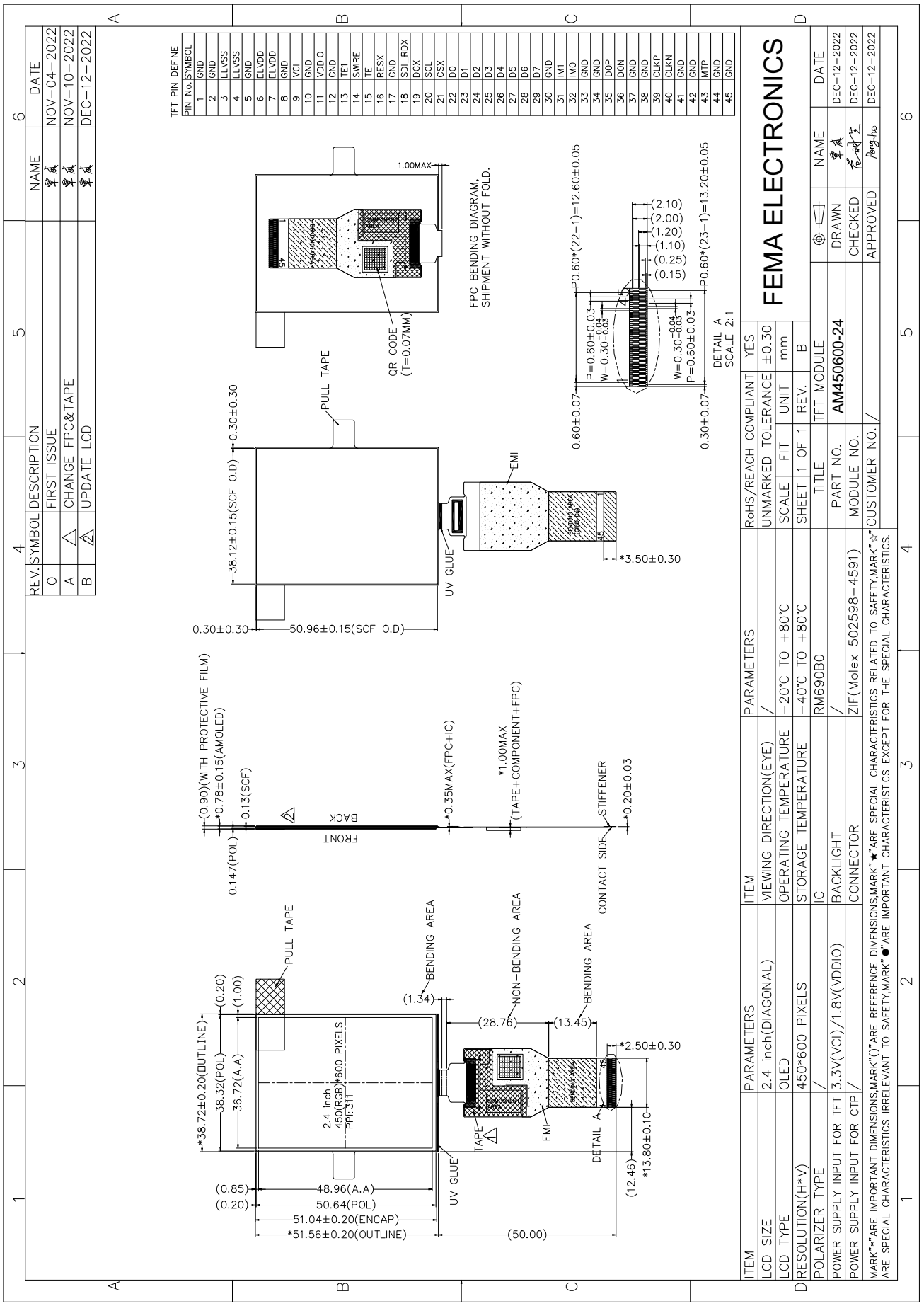
3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage	VDD	3.1	3.3	3.5	V	
I/O logic voltage	VDDIO	1.65	1.8	3.3	V	
OLED input Voltage	ELVDD	2.0	3.6	6	V	
OLED input Voltage	ELVSS	-4.7	-3.6	-0.4	V	
VCI_EN Voltage	VCI enable signal	VIL:0.4V VIH:1.2V				
Input voltage 'H' level	VIH	0.8VDDIO	-	VDDIO	V	
Input voltage 'L' level	VIL	VSS	-	0.2VDDIO	V	
Power supply current	IVDD	-	3	-	mA	
Frame Frequency(60Hz)	frame	58	60	62	HZ	
TFT gate on voltage	VGH	-	-	-	V	
TFT gate off voltage	VGL	-	-	-	V	
Analog power supply voltage	AVDD	-	-	-	V	
TFT common electrode voltage	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. VCOM must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

4. EXTERNAL DIMENSIONS



5. ELECTRO - OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time	Tr+ Tf	-	-	-	4	ms	FIG.1	Note 1
Contrast ratio	Cr		100000	-	-	-	FIG.2	Note 2
Surface luminance	Lv	θ=0°	720	800	-	cd/m^2	FIG.2	Note 3
Luminance uniformity	Yu	θ=0°	85	-	-	%	FIG.2	Note 4
NTSC	-	θ=0°	107	-	-	%	FIG.2	Note 5
Viewing angle	θ	∅=90°	80	-	-	deg	FIG.3	Note 6
		∅=270°	80	-	-	deg	FIG.3	
		∅=0°	80	-	-	deg	FIG.3	
		∅=180°	80	-	-	deg	FIG.3	
CIE (x,y) chromaticity	Red x	θ=0° ∅=0° Ta=25℃	Typ -0.04	0.68	Typ +0.04	-	FIG.2 CIE1931	Note 5
	Red y			0.31		-		
	Green x			0.24		-		
	Green y			0.72		-		
	Blue x			0.14		-		
	Blue y			0.05		-		
	White x			0.30		-		
	White y			0.30		-		

The TFT module should be stabilized at a given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.

Normally white:Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

Normally black:Rise time (T_{ON}) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 90% to 10%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10 angles are determined for the

horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the display surface. For more information see FIG.3.
For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on CS-2000/BM-7 photo detector or compatible.

FIG.1. The definition of response Time

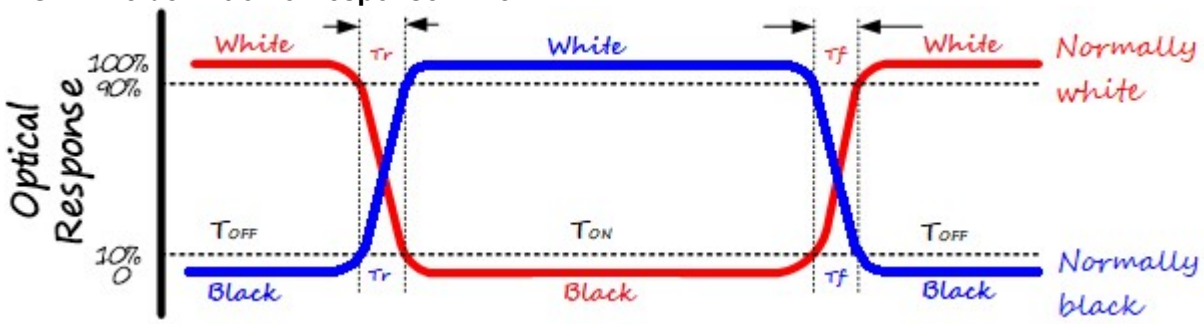


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area
Light spot size ∅=1.5mm or ∅=7.7mm (CS-2000/BM-7)50cm distance or compatible distance from the LCM surface to detector lens.
Test spot position : see Figure a.
measurement instrument : Luminance meter CS-2000/BM-7 or compatible ,see Figure b.

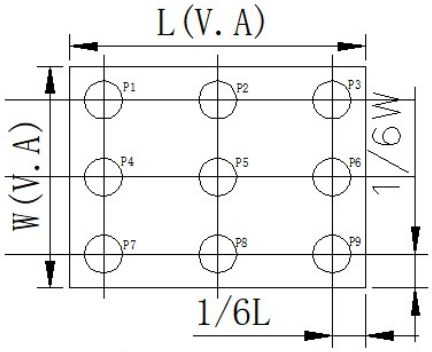


Figure a

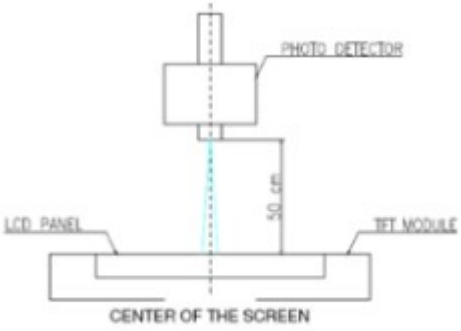
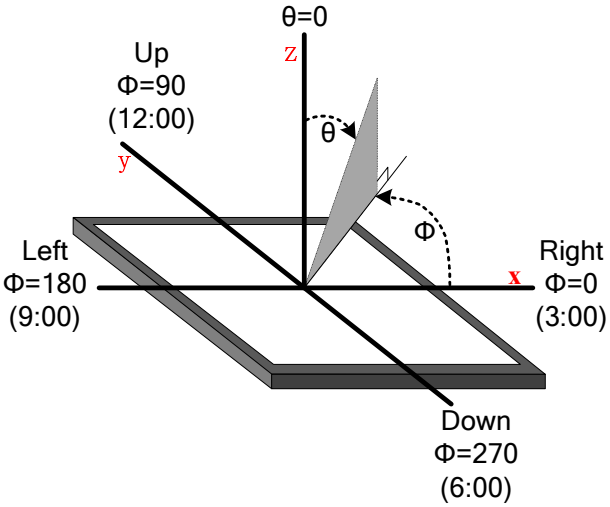


Figure b

FIG.3. The definition of viewing angle



6. INTERFACE DESCRIPTION

Module Interface description

Interface No.	Name	I/O or connect to	Description
1-2	GND	P	Ground
3-4	ELVSS	P	Negative Power supply for Panel
5	GND	P	Ground
6-7	ELVDD	P	Positive Power supply for Panel
8	GND	P	Ground
9	VCI	P	Power supply for display driver IC analog system
10	GND	P	Ground
11	VDDIO	P	Power supply for display driver IC interface and logic system
12	GND	P	Ground
13	TE1	O	IC Status active reporting pin
14	SWIRE	O	Swire protocol setting pin of Power IC
15	TE	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low
16	RESX	I	Display driver reset, must be applied to properly initialize the chip. Signal is active low
17	GND	P	Ground
18	SDI_RDX	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX: Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface
19	DCX	I	Display data / command selection in 80-series MCU I/F and 4-wire SPI I/F
20	SCL	I	WRX : Writes strobe signal to write data when WRX is “Low” in 80-series MCU I/F. SCL: A synchronous clock signal in SPI I/F
21	CSX	I	Chip select input pin (“Low” enable) in 80-series MCU I/F and SPI I/F
22-29	D0-D7	I/O	8-bit bi-directional data bus for 80-series MCU I/F and 8-bit input data bus for RGB I/F
30	GND	P	Ground
31	IM1	I	Interface type selection
32	IM0		
33-34	GND	P	Ground
35	D0P	I/O	Differential data signals if MIPI interface.
36	D0N	I/O	Differential data signals if MIPI interface.
37-38	GND	P	Ground
39	CLKP	I	Differential clock signals if MIPI interface
40	CLKN	I	Differential clock signals if MIPI interface.
41-42	GND	P	Ground
43	MTP	P	MTP programming power supply. Must be left open or connected to GND in normal condition
44-45	GND	P	Ground

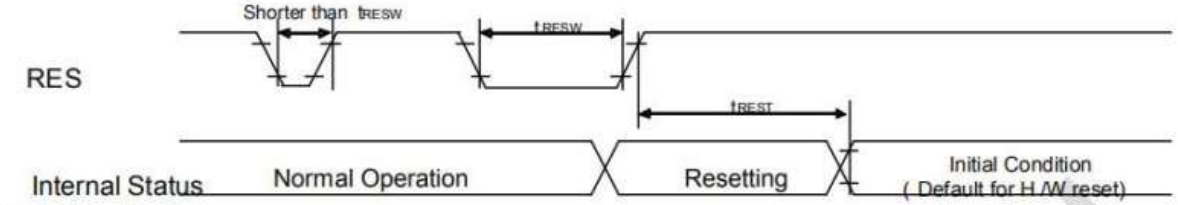
I: input, O: output, P: Power,NC or / : No connection

7.AC CHARACTERISTICS

TFT Module AC CHARACTERISTICS

Reset Timing Sequence Requirement

Display panel reset timing:



Reset input timing:

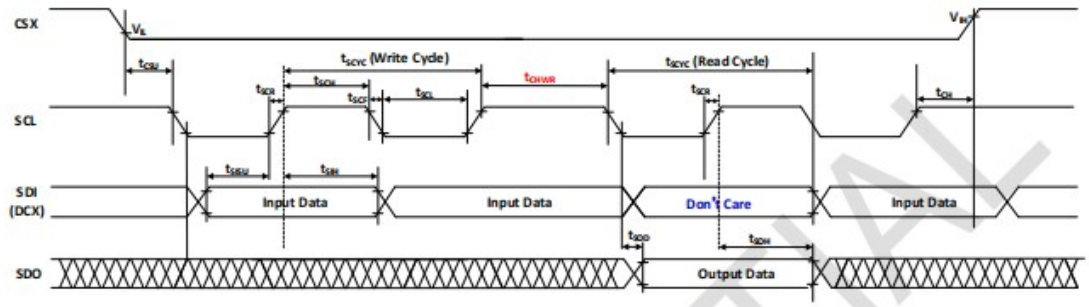
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	30	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	20	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Communication Interface timing

SPI/DUAL-SPI Characteristics

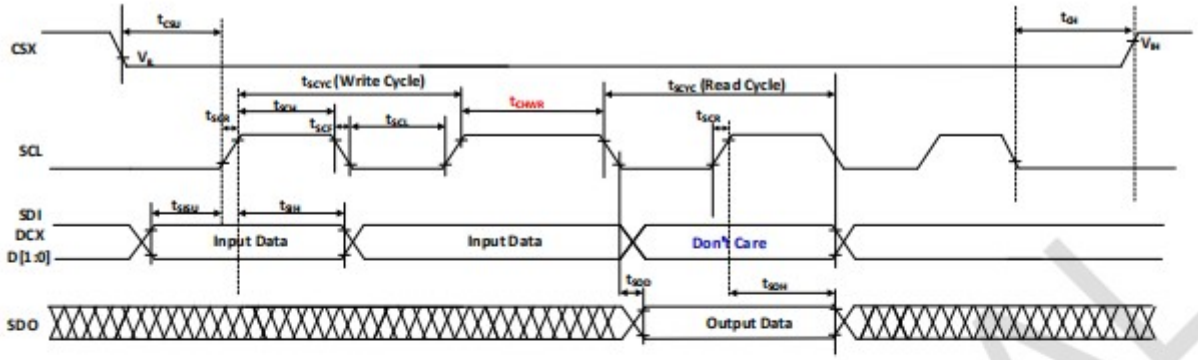
3/4-wire SPI



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	20			ns
		Read	300			ns
Clock high pulse width	t_{SCH}	Write	6.5			ns
	t_{SCH}	Read	140			ns
Clock low pulse width	t_{SCL}	Write	6.5			ns
	t_{SCL}	Read	140			ns
Clock rise time	t_{SCR}	0.2*VDDI -> 0.8*VDDI			3.5	ns
Clock fall time	t_{SCF}	0.8*VDDI -> 0.2*VDDI			3.5	ns
Chip select setup time	t_{CSU}		10			ns
Chip select hold time	t_{CH}		10			ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge	5			ns
Data input hold time	t_{SIH}		5			ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge			120	ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge	150			ns

Notes:
(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.
(2) For the 4-wire SPI, the DCX's timing is the same as input data.
(3) Ta = -30℃ to 70℃, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, and VSS=0V

QUAD-SPI Characteristics



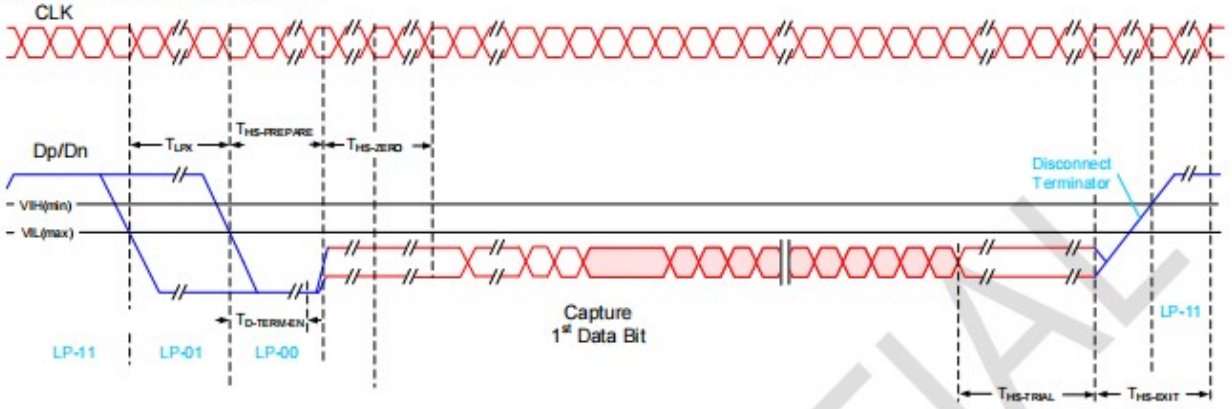
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	tSCYC	Write	20			ns
		Read	150			ns
Clock high pulse width	tSCH	Write	6.5			ns
	tSCH	Read	70			ns
Clock low pulse width	tSCL	Write	6.5			ns
	tSCL	Read	70			ns
Clock rise time	tSCR	0.2*VDDI -> 0.8*VDDI			3.5	ns
Clock fall time	tSCF	0.8*VDDI -> 0.2*VDDI			3.5	ns
Chip select setup time	tCSU		20			ns
Chip select hold time	tCH		20			ns
Data input setup time	tSISU	To VIL of SCL's rising edge	4			ns
Data input hold time	tSIH		4			ns
Access time of output data	tSOD	From VIL of SCL's falling edge			70	ns
Hold time of output data	tSOH	From VIH of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	tCHWR	From VIH of SCL's rising edge	150			ns

Note: The max SCL frequency for each pixel data format is specified as the below table.
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, GND=0V
Note: 4-wire QSPI support transfer rate in pixel data write

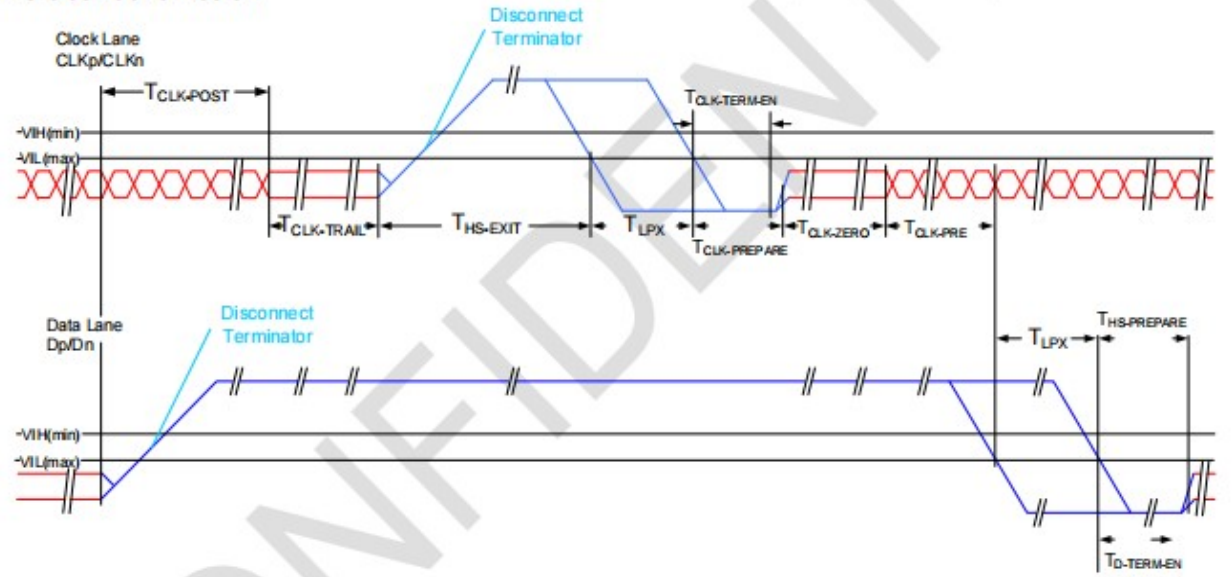
		4-wire QSPI suppor transfer rate
Pixel Data Write	RGB888	50MHz
	RGB666	50MHz
	RGB565	50MHz

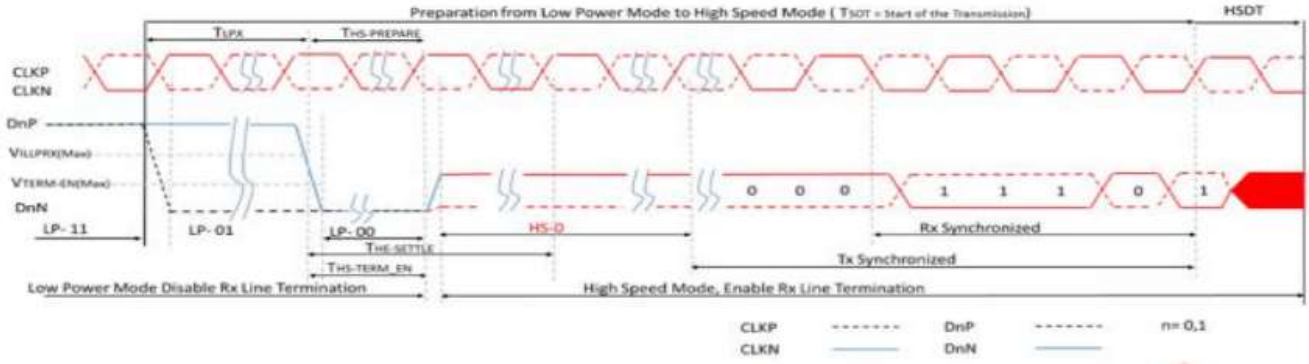
DSI Timing Characteristics

HS Data Transmission Burst



HS clock transmission





Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from Low Power Mode to High Speed Mode Timing

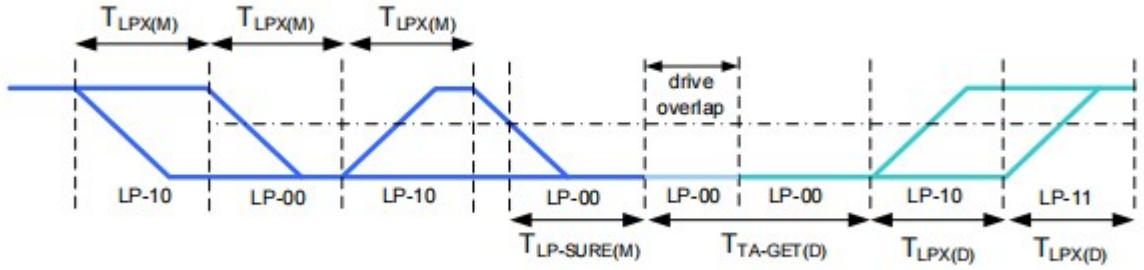
Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	TLPX	Length of any Low Power State Period	50			nS	1
DnP/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0, and 1*

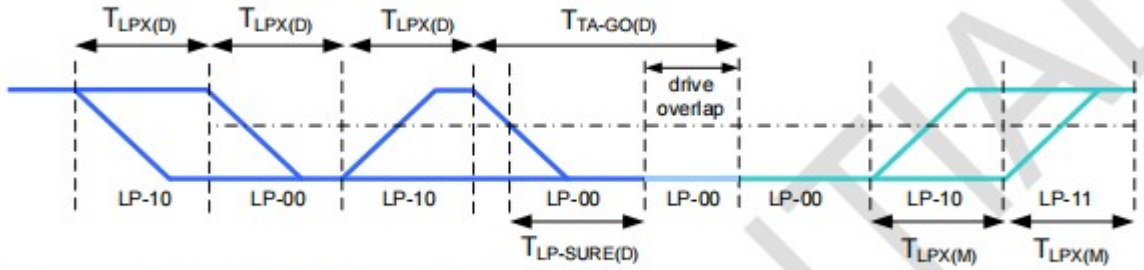
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

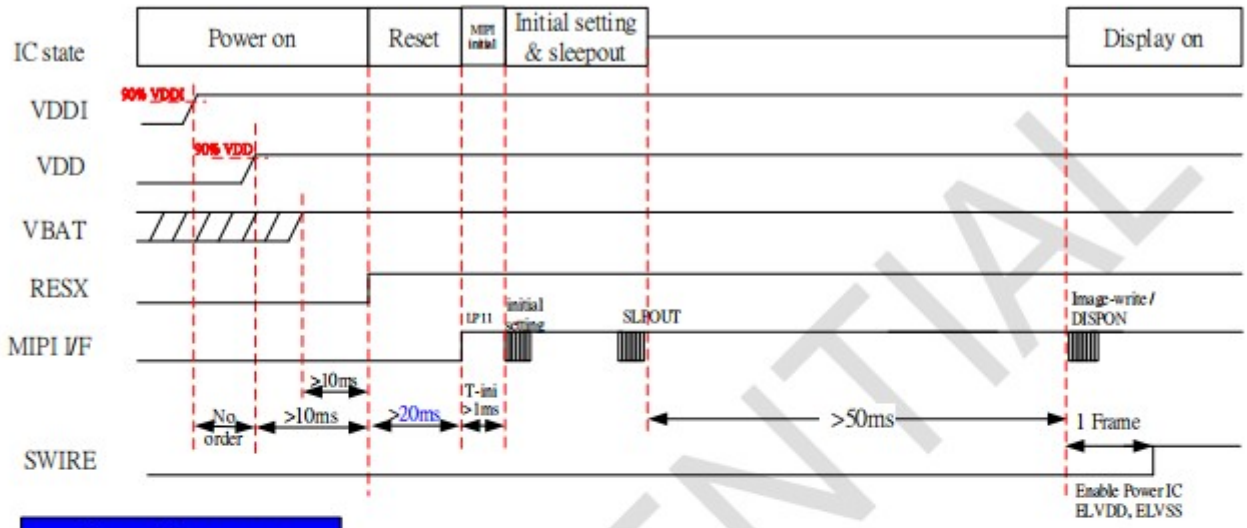
Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

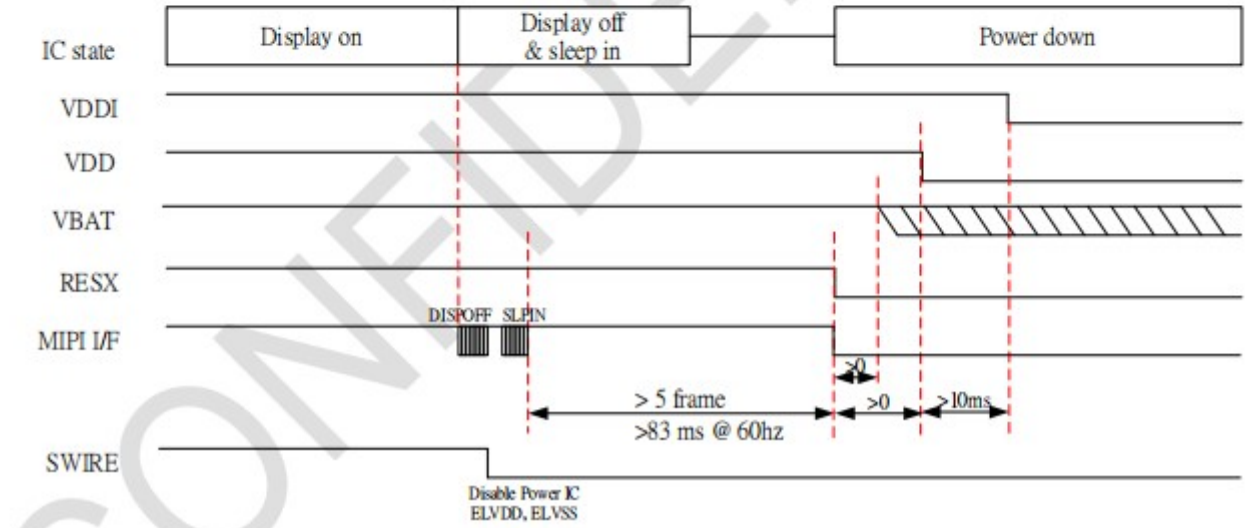
8. POWER SEQUENCE

To prevent the device damage from latch up and Improve subjective display effect,the power ON/OFF sequence shown below must be followed.

Power On sequence



Power Off sequence



9. RELIABILITY TEST CONDITIONS

<table>
<tr><th>No.</th><th>Test item</th><th colspan="2">Test condition</th><th>Inspection after test</th></tr>
<tr><td>9.1</td><td>High temperature storage test</td><td colspan="2">+80℃/240 hours</td><td rowspan="11">Inspection after 2~4hours storage at room temperature, the sample should not have following defects:
1.Current changing value before test and after test is 50% larger;
2. Function defect : Non-display,abnormal-display,missing lines, Short lines,ITO corrosion;
3.Visual defect : Air bubble in the LCD,Seal leak,Glass crack.</td></tr>
<tr><td>9.2</td><td>Low temperature storage test</td><td colspan="2">-40℃/240 hours</td></tr>
<tr><td>9.3</td><td>High temperature operating test</td><td colspan="2">+80℃/240 hours</td></tr>
<tr><td>9.4</td><td>Low temperature operating test</td><td colspan="2">-20℃/240 hours</td></tr>
<tr><td>9.5</td><td>Thermal Shock
(non-operation)</td><td colspan="2">-40℃ ←→ +80℃/80cycles
(30min.)(<30sec.) (30min.)</td></tr>
<tr><td>9.6</td><td>High temperature high humidity test</td><td colspan="2">+60℃*90% RH/240 hours</td></tr>
<tr><td>9.7</td><td>Vibration test for Packaging</td><td colspan="2">Frequency : 250 r/min
Amplitude : 1 inch
Time: 45min</td></tr>
<tr><td rowspan="5">9.8</td><td rowspan="5">Drop test for Packaging</td><td colspan="2">Drop direction:
1 corner/3 edges/6 sides 10 times</td></tr>
<tr><td>Packing weight(kg)</td><td>Drop height(cm)</td></tr>
<tr><td>〈11</td><td>80±1.6</td></tr>
<tr><td>11≦G〈21</td><td>60±1.2</td></tr>
<tr><td>21≦G〈31</td><td>50±1.0</td></tr>
<tr><td>9.9</td><td>ESD test</td><td colspan="2">Air discharge: TBD
Contact discharge:TBD</td></tr>
</table>

Remark :
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 3~5pcs.
3.For High temperature high humidity test, Pure water(Resistance>10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5.Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic.
6.After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

10.INSPECTION CRITERION

TBD

11. HANDLING PRECAUTIONS

11.1 Mounting method

The TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.
Extreme care should be needed when handling the TFT modules.

11.2 Caution of TFT module handling and cleaning

When cleaning the display surface, Use soft cloth with solvent
[recommended below] and wipe lightly :
●.Isopropyl alcohol
●.Ethyl alcohol
Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent :
●.Water
●.Aromatics
Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns
Do not use the following solvent on the pad or prevent it from being contaminated :
●.Soldering flux
●.Chlorine (Cl) , Sulfur (S)
If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.
If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

11.3 Caution against static charge

The TFT module use C-MOS LSI drivers, so we recommended that you :
Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

11.4 Packing

Module employ TFT elements and must be treated as such.
●.Avoid intense shock and falls from a height.
●.To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

11.5 Caution for operation

●.It is an indispensable condition to drive TFT module within the specified voltage limit since the higher voltage then the limit cause the shorter TFT module life.
●.An electrochemical reaction due to direct current causes TFT module undesirable deterioration, so that the use of direct current drive should be avoided.
●.Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature TFT module how dark color in them. However those phenomena do not mean malfunction or out of order with TFT module, which will come back in the specified operation temperature.
●.If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
●.A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
●.Usage under the maximum operating temperature, 50%Rh or less is required.
●.When fixed patterns are displayed for a long time,remnant image is likely to occur.

11.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.
●.Storing in an ambient temperature 10℃ to 30℃, and in a relative humidity of 45% to 75%. Don't expose to sunlight or fluorescent light.
●.Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
●.Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature

range.
●.Storing with no touch on polarizer surface by the anything else.
It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

11.7 Safety

●.It is recommendable to crash damaged or unnecessary TFT module into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
●.When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

12. PRECAUTION FOR USE

12.1 A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.
12.2 On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.
●.When a question is arisen in this specification.
●.When a new problem is arisen which is not specified in this specifications.
●.When an inspection specifications change or operating condition change in customer is reported to FEMA, and some problem is arisen in this specification due to the change.
●.When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

13. PACKING SPECIFICATION

Please consult our technical department for detail information.

14. INITIALIZATION CODE

```
MIPI_SPI3_Write_GP_COMD_DATA(2);
SPI3_DAT_8bit(0xFE);
SPI3_DAT_8bit(0x00);

MIPI_SPI3_Write_GP_COMD_DATA(5);
SPI3_DAT_8bit(0x2A);
SPI3_DAT_8bit(0x00);
SPI3_DAT_8bit(0x10);
SPI3_DAT_8bit(0x01);
SPI3_DAT_8bit(0xD1);

MIPI_SPI3_Write_GP_COMD_DATA(5);
SPI3_DAT_8bit(0x2B);
SPI3_DAT_8bit(0x00);
SPI3_DAT_8bit(0x00);
SPI3_DAT_8bit(0x02);
SPI3_DAT_8bit(0x57);

MIPI_SPI3_Write_GP_COMD_DATA(2);
SPI3_DAT_8bit(0x35);
SPI3_DAT_8bit(0x00);

MIPI_SPI3_Write_GP_COMD_DATA(2);
SPI3_DAT_8bit(0xC2);
SPI3_DAT_8bit(0x00);

MIPI_SPI3_Write_GP_COMD_DATA(2);
SPI3_DAT_8bit(0x51);
SPI3_DAT_8bit(0xFF);
```

```
MIPI_SPI3_Write_GP_COMD_DATA(1);
SPI3_DAT_8bit(0x11);
delay_ms(120);

MIPI_SPI3_Write_GP_COMD_DATA(1);
SPI3_DAT_8bit(0x29);
delay_ms(120);
```

15. HSF COMPLIANCE

●.This products complies with ROHS 2011/65/EU and 2015/863/EU、REACH 1907/2006/EC requirements, and the packaging complies with 94-62-EC.