DATASHEET

11/7/2013

Fema Part Number

GM800600A-121-TTX2NLW-H1	
Description	12.1" Full Color TFT Display (Rev 1)
	800x600 Resolution
	Brightness = 1000 nits (Typical)
	Optional Resistive or Projected Capacitive Touch Panel Available

Fema Electronics Corporation:

17815 Newhope Street, Suite H, Fountain Valley, CA 92708 Tel: 714-825-0140

Please visit our website www.femaelectronics.com or email us at tft@femacorp.com

2. General Description

2.1, Overview

This specification applies to the 12.1 inch color TFT-LCD module with brightness enhanced backlight and 1-ch LVDS interface. The screen format is intended to support SVGA (800(H) x 600(V)) screen and 16.2M (RGB 8-bits) or 262K colors (RGB 6-bits). All input signals are LVDS interface compatible. The LED driver is not included.

2.2 Features

- Sunlight readable display, 800nits.
- LED backlight
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial Application; especial kiosk and digital signage display.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	inch	12.1
Active Area	mm	246.0(H) x 184.5(V)
Pixels H x V	pixels	800x3(RGB) x 600
Pixels Pitch	um	307.5 (per one triad) x 307.5
Pixel Arrangement		RGB Vertical stripe
Display mode		TN mode, normally white
White luminance (center)	Cd/m^2	1000 (Typ.)
Contrast ratio		600 (Typ.)
Optical Response Time	msec	35 ms (Typ. on/off)
Normal Input Voltage VDD	Volt	3.3
Power Consumption (VDD Line + LED backlight)	Watt	8.4 (VDD 1.0W ; LED 7.4W
Weight	Grams	580 max.
Physical size	mm	279.0(H)x 209.0(V) x 9.0(D) (typ.)
Electrical Interface		One Chanel LVDS
Support Colors		16.2 M colors (RGB 8-bits)
Surface Treatment		Anti-Glare, 3H
Temperature range Operating Storage (Shipping)	 ^0C ^0C	 -30 ~ 85(LCD surface temperature) -30 ~ 85
RoHS Compliance		RoHS Compliance

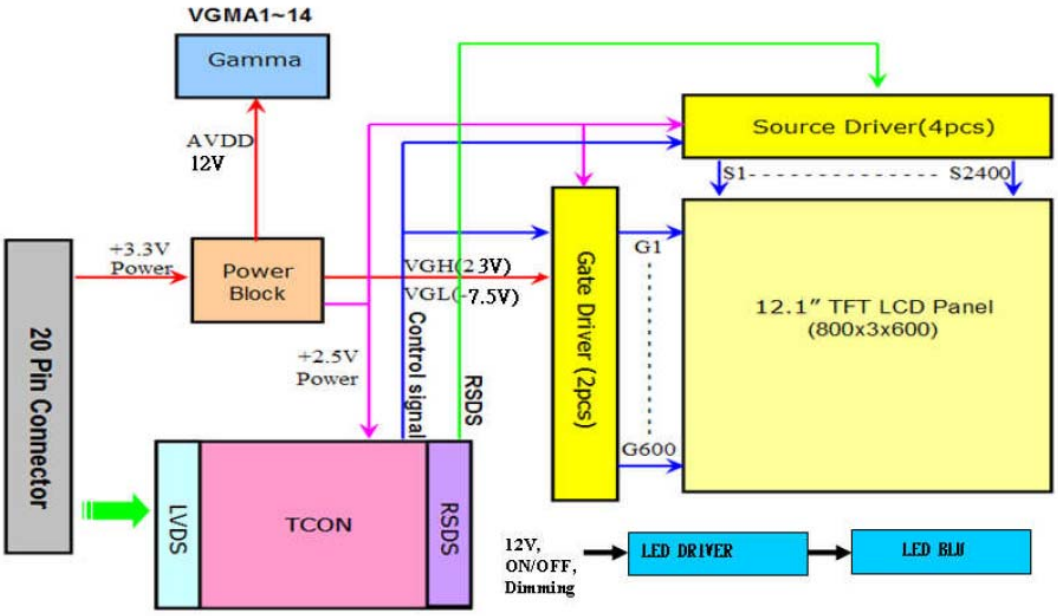
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	70	80		2
		CR=10 (Left)	70	80		
		Vertical (Up)	55	65		
		CR=10 (Down)	65	75		
Contrast Ratio		Normal Direction	400	600		3
Response Time	msec	Raising time (T_{rR})		10	20	4
		Falling time (T_{rF})		25	30	
		Raising + Falling		35	50	
Color / Chromaticity Coordinates (CIE)		Red x	-0.03	0.60	+0.03	5
		Red y		0.35		
		Green x		0.33		
		Green y		0.61		
		Blue x		0.16		
		Blue y		0.09		
Color coordinates (CIE) White		White x		0.313		
		White y		0.329		
Center Luminance	Cd/m^2		650	800		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

3. **Functional Block Diagram**

The following diagram shows the functional block of the 12.1 inches Color TFT-LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Logic/ LCD drive voltage	Vin	-0.3	3.6	Volt	Note 1, 2

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED	--	640	mA	Note 1, 2

4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-30	-	85	^{0}C	Note 3
Operation Humidity	H_{OP}	5		90	%	
Storage temperature	T_{ST}	-30		85	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

5. Electrical characteristics

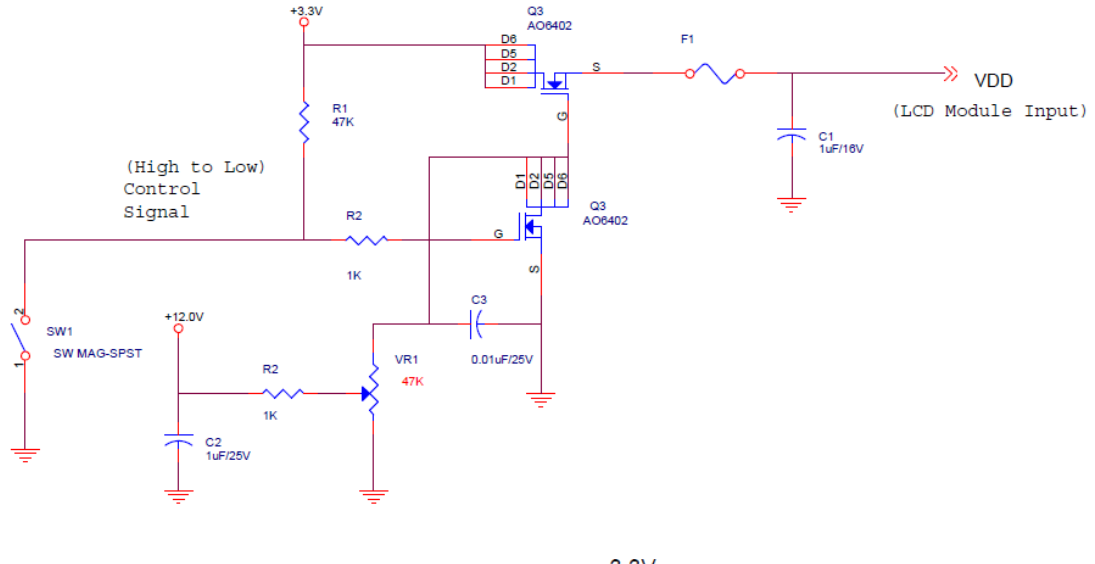
5.1 TFT LCD Module

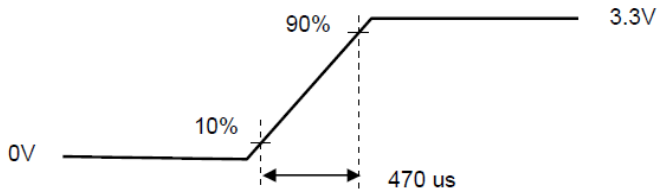
5.1.1 Power Specification

Input power specifications are as follows

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
VDD	Logic/ LCD Drive Voltage	3	3.3	3.6	Volt	+/- 10%
IDD	Input current		285		mA	VDD=3.3V, All black pattern.
PDD	VDD power		0.94		W	VDD=3.3V, All black pattern.
IRush	Inrush current			1.5	A	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mV p-p	VDD=3.3V, All black pattern.

Note 1: Measurement condition:





VDD rising time

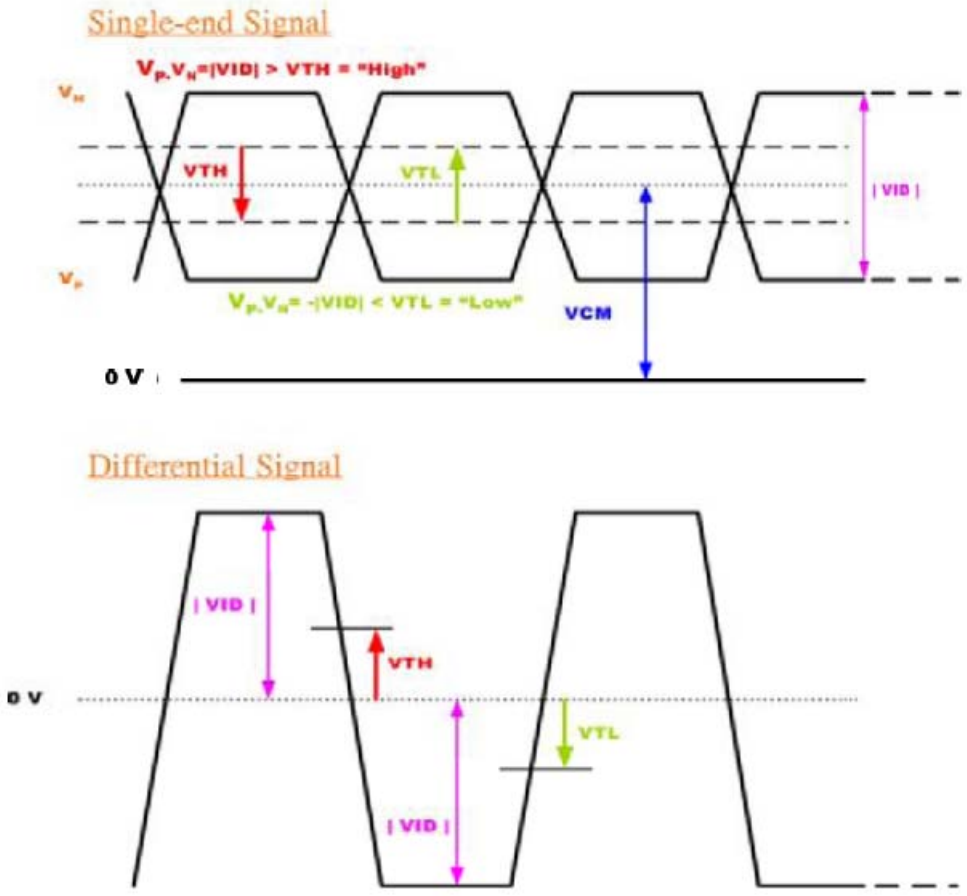
5.1.2 Signal Electrical Characteristics

Input signal shall be low or Hi-Z state when VDD is off. Please refer to specification of SN75LVDS82DGG (Texas Instruments) in detail.

Characteristics of each signal are as following:

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VTH	Differential Input High Threshold			+100	mV	VICM = 1.2V
VTL	Differential Input Low Threshold	-100			mV	VICM = 1.2V
|VID|	Input Differential Voltage	100	400	600	mV	
VICM	Differential Input Common Mode Voltage	+1.1		+1.45	V	VTH/VTL = 100mV

Note: LVDS Signal Waveform.



5.2 Backlight Unit

Parameter guideline is under stable conditions at 25℃ (Room Temperature):

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		19.8		[V]	2
LED current (IL)		380		[mA]	2,
LED Life Time(LTLED)		50,000		[Hour]	1

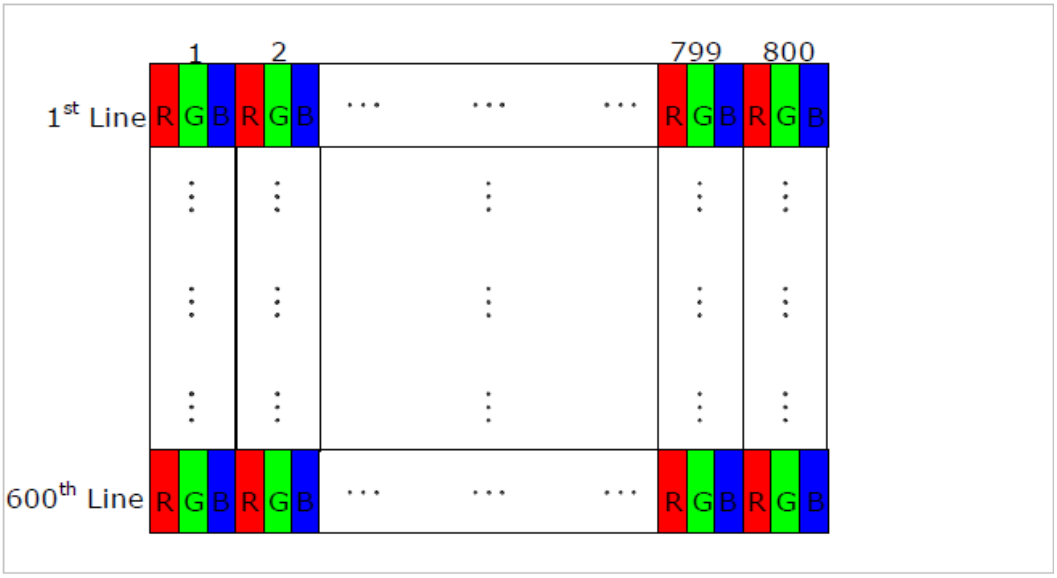
Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 380 mA.

Note 2: The LED driving condition is defined for each LED module.(8 LED Serial, a LED includes 6 Chips)

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.3 TFT-LCD Interface Signal Description

The module using a LVDS receiver embedded in ASIC. LVDS is a differential signal technology for LCD interface and a high-speed data transfer device.

Input Signal Interface		
Pin No.	**Symbol**	**Description**
1	VDD	Power Supply, 3.3V (typical)
2	VDD	Power Supply, 3.3V (typical)
3	GND	Ground
4	SEL68	6/ 8bits LVDS data input selection [H: 8bits L/NC: 6bit]
5	RIN0-	LVDS receiver signal channel 0
6	RIN0+	LVDS Differential Data Input (R0, R1, R2, R3, R4, R5, G0)
7	GND	Ground
8	RIN1-	LVDS receiver signal channel 1
9	RIN1+	LVDS Differential Data Input (G1, G2, G3, G4, G5, B0, B1)
10	GND	Ground
11	RIN2-	LVDS receiver signal channel 2
12	RIN2+	LVDS Differential Data Input (B2, B3, B4, B5, HS, VS, DE)
13	GND	Ground
14	CLKIN-	LVDS receiver signal clock
15	CLKIN+	
16	GND	Ground
17	RIN3-	LVDS receiver signal channel 3, NC for 6 bit LVDS Input
18	RIN3+	LVDS Differential Data Input (R6, R7, G6, G7, B6, B7, RSV)
19	RSV	Reverse Scan Function [H: Enable; L/NC: Disable]
20	NC/GND	Reserved for internal test. Please treat it as NC.

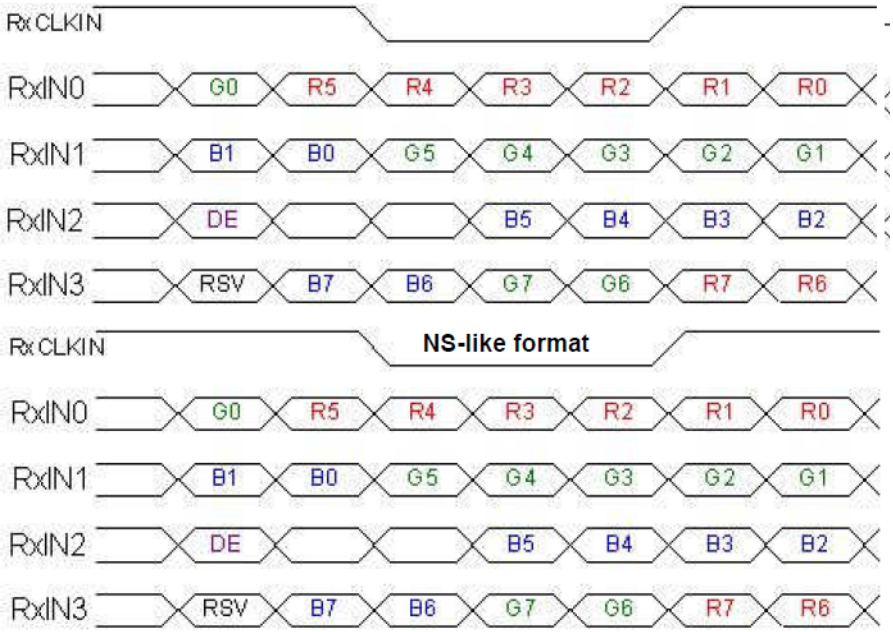
Note 1: Input Signals shall be in low status when VDD is off.

Note 2: High stands for “3.3V”, Low stands for “0V”, NC stands for “No Connection”.

Note 3: RSV stands for “Reserved”.

6.4 LVDS Signal Format:

6.4.1SEL68



Note1: Please follow PSWG. **Note2**: R/G/B data 7:MSB, R/G/B data 0:LSB

Signal Name	Description	
+RED5(R5) +RED4(R4) +RED3(R3) +RED2(R2) +RED1(R1) +RED0(R0)	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN5(G5) +GREEN4(G4) +GREEN3(G3) +GREEN2(G2) +GREEN1(G1) +GREEN0(G0)	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE5(B5) +BLUE4(B4) +BLUE3(B3) +BLUE2(B2) +BLUE1(B1) +BLUE0(B0)	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
CLK	Data Clock	The typical frequency is 40MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of CLK. When the signal is high, the pixel data shall be valid to be displayed.

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.5 Interface Timing

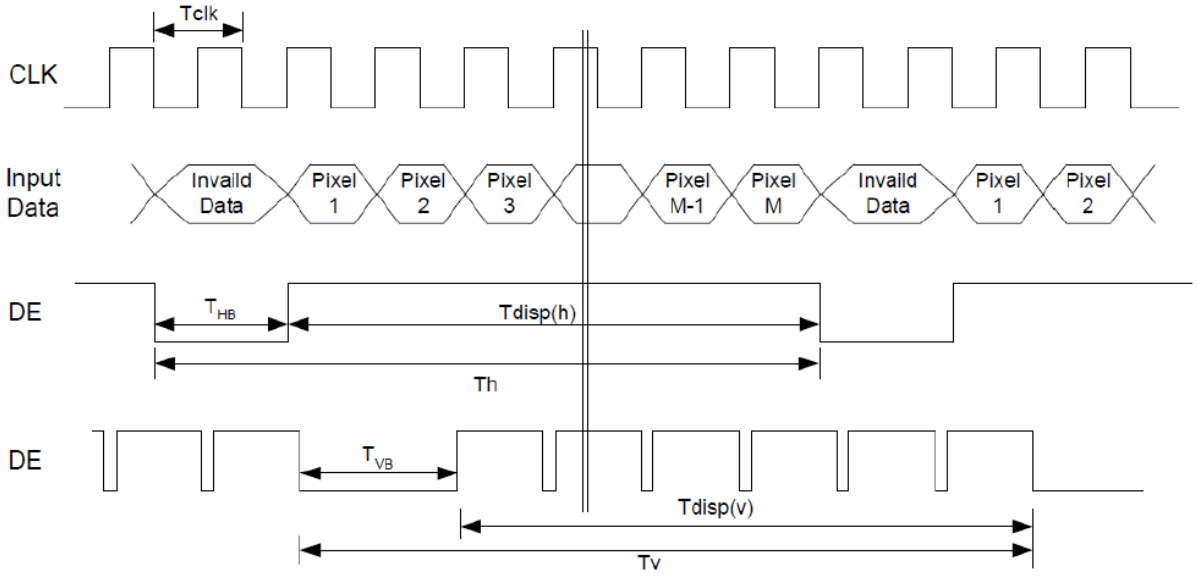
6.5.1 Timing Characteristics

Signal		Symbol	Min.	Typ.	Max.	Unit
Clock Frequency		1/ T_{Clock}	34	40	48.3	MHz
Vertical Section	Period	T_V	608	628	1024	T_{Line}
	Active	T_{VD}	--	600	--	
	Blanking	T_{VB}	8	28	423	
Horizontal Section	Period	T_H	960	1056	1060	T_{Clock}
	Active	T_{HD}	--	800	--	
	Blanking	T_{HB}	220	256	440	

Note1: Frame rate is 60 Hz.

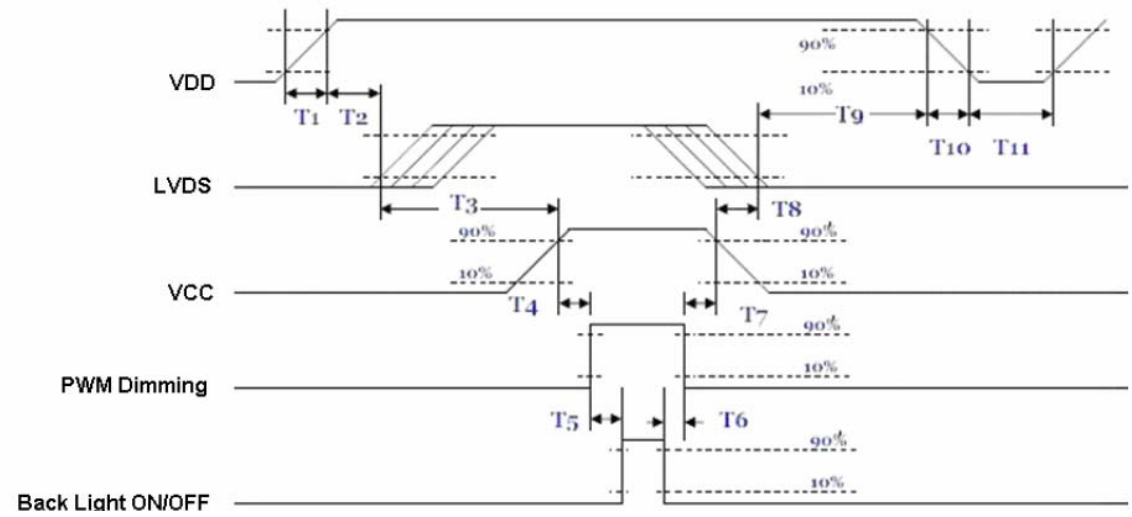
Note2: DE mode only

6.5.2 Input Timing Diagram



6.6 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as below. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power ON/OFF sequence timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	30	40	50	[ms]
T3	200	-	-	[ms]
T4	10	-	-	[ms]
T5	10	-	-	[ms]
T6	0	-	-	[ms]
T7	10	-	-	[ms]
T8	100	-	-	[ms]
T9	0	16	50	[ms]
T10	-	-	10	[ms]
T11	1000	-	-	[ms]

The above on/off sequence should be applied to avoid abnormal function in the display. Please make sure to turn off the power when you plug the cable into the input connector or pull the cable out of the connector.

7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	STM
Type Part Number	MSB240420-E
Mating Housing Part Number	P240420 or compatible

Pin No.	Symbol	Pin No.	Symbol
1	VDD	2	VDD
3	GND	4	SEL68
5	RIN0-	6	RIN0+
7	GND	8	RIN1-
9	RIN1+	10	GND
11	RIN2-	12	RIN2+
13	GND	14	CLKIN-
15	CLKIN+	16	GND
17	RIN3-	18	RIN3+
19	RSV	20	NC/GND

7.2 Backlight Unit

Recommended connector : JOIN TEK JT1025-1021

Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	

8. Reliability Test

Environment test conditions are listed as following table.

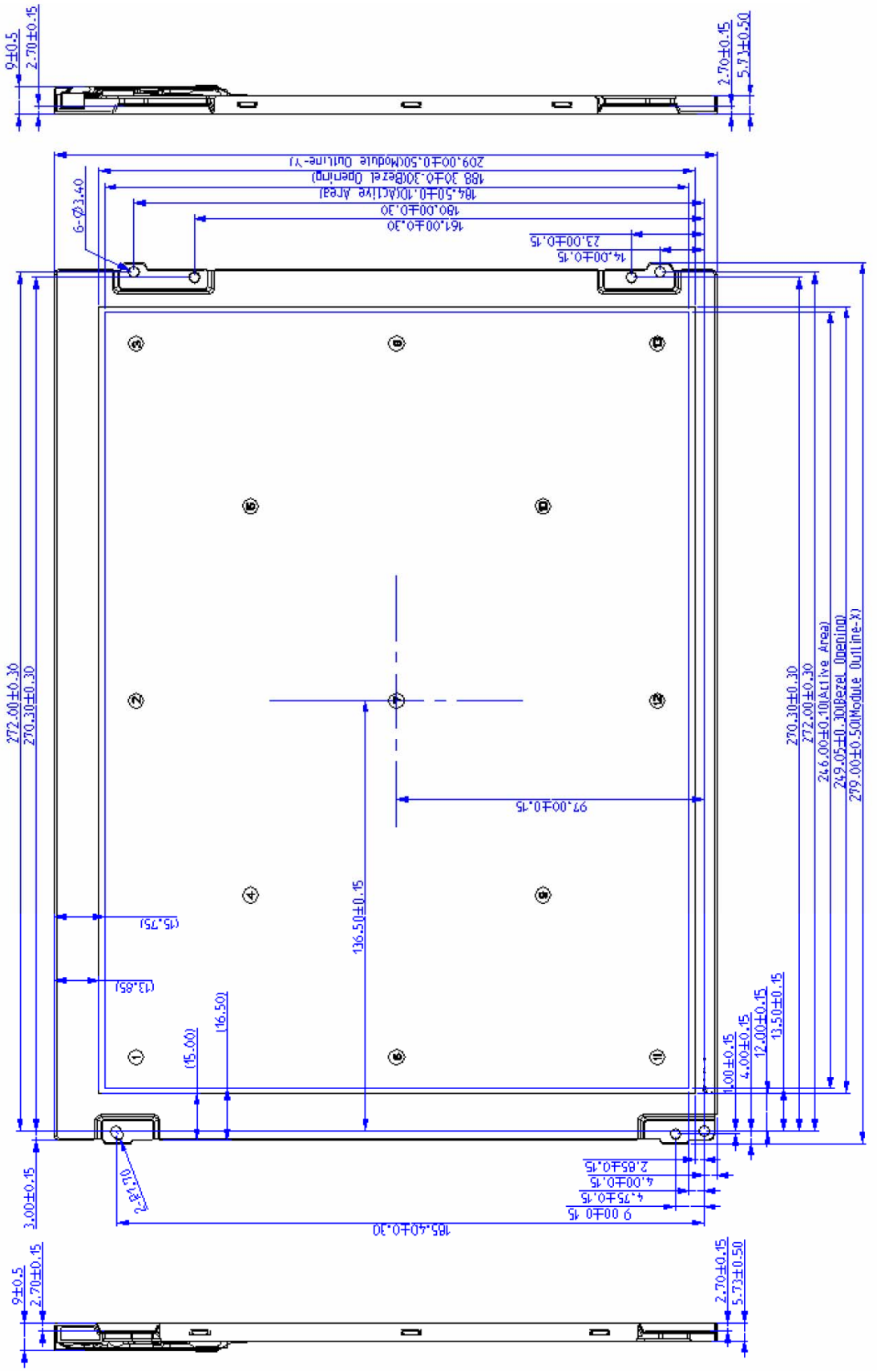
Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 90%RH, 240hours	
High Temperature Operation (HTO)	Ta= 85℃, 50%RH, 240hours	3
Low Temperature Operation (LTO)	Ta= -30℃, 240hours	
High Temperature Storage (HTS)	Ta= 85℃, 240hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

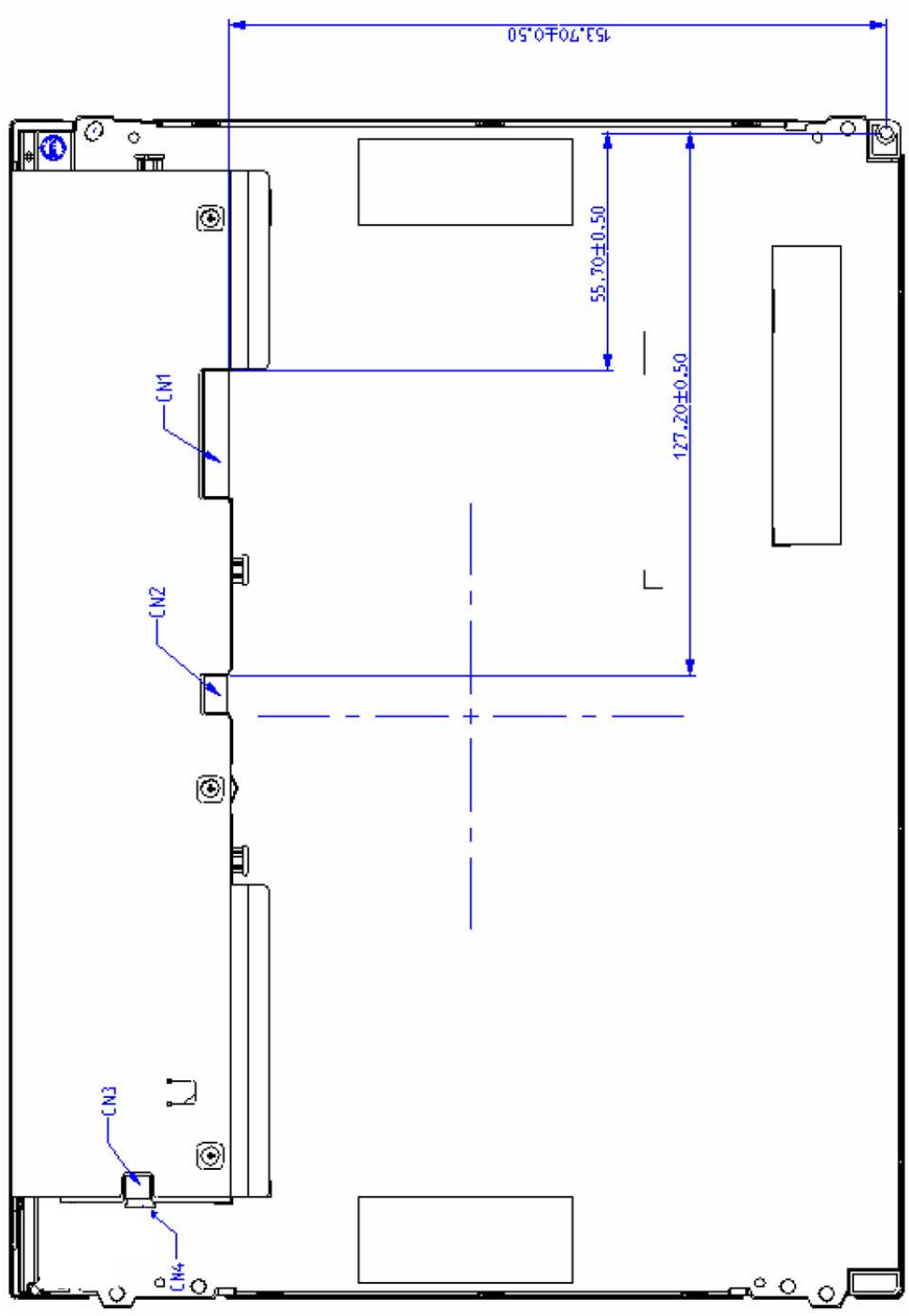
Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

10. Mechanical Characteristic





(Note: The LED line is not shown)